Amendments to the Specification:

Please replace the paragraph beginning on page 1, line 4, with the following amended paragraph:

Magnetic Random Access Memories ~~(MRAN)~~ (MRAM) offer many advantages over existing RAM technologies: With MRAM, it is claimed to reach the writing and reading speed of Static RAM (SRAM), the density of Dynamic RAM (DRAM) and the non-volatility of Flash Memory.

Please replace the paragraph beginning on page 4, line 30, with the following amended paragraph:

A further preferred embodiment of the invention comprises ~~read~~ a read controller connected with the register and the memory. The read controller is adapted to

- receive a read request comprising the first address information
- ascertain whether the first address information is stored in the register
- forward the read request to the register or the memory, depending on whether or not, respectively, the first address information is stored in the register. The memory manager of this embodiment provides the advantages of the register also read operations from the memory. It makes sure, that upon a read request the latest data always allocated to the address information given in the read request is returned to the client that originated the read request. That address information is called first address information for reasons of simplicity as well. It is obvious, however, that a write request may be directed to a different address in a memory than a read request.

Please replace the paragraph beginning on page 5, line 15, with the following amended paragraph:

In a further preferred embodiment of the memory controller of the invention the write controller is additionally adapted to

- allocate a flag indicative of the result of the comparison to said first write data and
- to transfer the flag to said register along with said first write data and said first address information, and to
- initiate a write operation to the memory only for first write data for which the flag is indicative of a difference between said first write data and said memory data or said second write data, respectively. In this embodiment, a data structure comprising three components is written to the register: the first component is the first address information, the second component is the first write data, and the third component is the flag allocated to the first write data. The flag indicates whether the first write data is to be written to the memory or not. As an example, let the flag be a "1" for a first case in which the comparison showed that the first write data is different from the memory data or the second write data, respectively, and "0" in the second case, that is if not different. In a queue type register, when the first write data is the oldest data in the register, the ~~writer~~ write controller will check the flag and perform the write operation to the memory only if the flag is in the state "1". In any case, the first write data will be replaced in the register by the next oldest write request data.

Please replace the paragraph beginning on page 8, line 1, with the following amended paragraph:

The present memory controller has the advantage that it is simpler and therefore faster than the memory controller described above. The cost of this advantage is that there will be first and second write requests to the same memory address in the register comprising identical write data for a memory cell or a group of memory cells. This means that these memory cells ~~will be~~ will first be overwritten when the write operation

for the first write request is performed, and then again with the same data when the second write request is served. However, the number of these events is generally not so large.